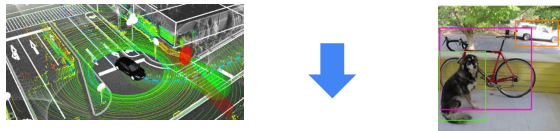


Project Challenge

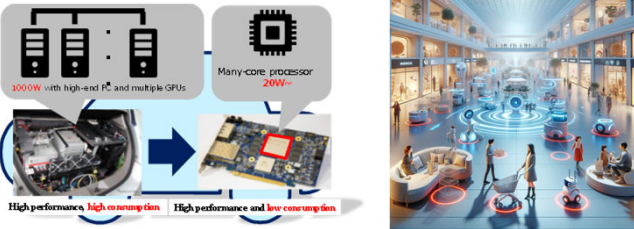
Many-Core Processor Utilization in Mobility

- Building out a robust middleware infrastructure compatible with **ROS 2 for many-core processors**
- Establishing a **model-based development** paradigm for many-core environments that balances **parallel computing** with **high productivity** demands



Intellectual Merit

The construction of ICT infrastructure software that makes effective use of **many cores** and takes into account the **scale, power saving, and real-time performance**



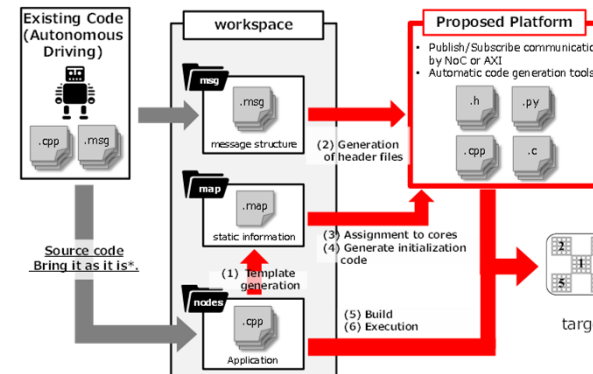
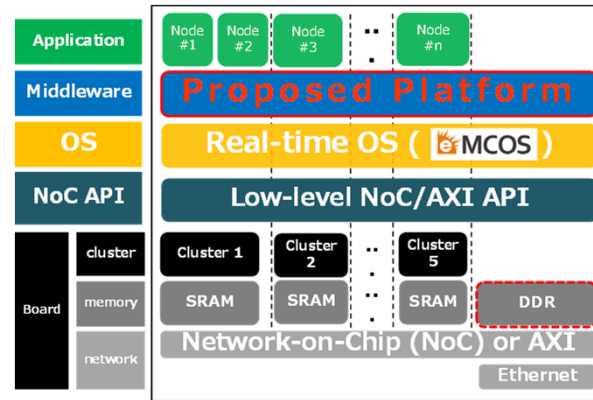
	Multi-core	Many-core	Non-Cluster	Cluster
Memory Architecture	Router	Router	NoC Architecture	NoC Architecture
Bus connection	Bus connection	Network-on-Chip (NoC)	Network-on-Chip (NoC)	Network-on-Chip (NoC)
Number of cores	2~16 cores	64 cores or more	✓	✓
Programmability			✓	✓
Scalability			✓	✓

Hardware Resource Comparison (CPU/GPU/FPGA/Many core)

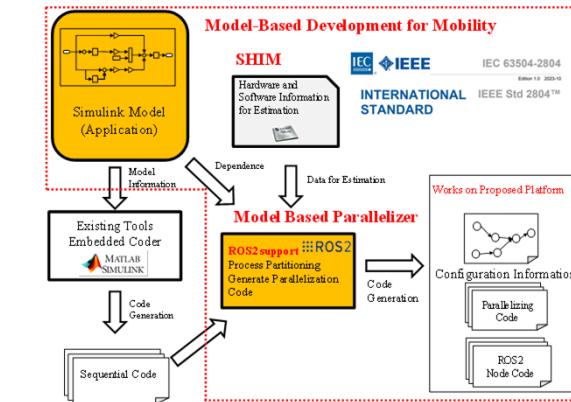
Hardware Resource	Purpose	Peak Performance	Energy Efficiency	Productivity
CPU	GP	Bad	Fair	Superior
GPU	IMG/DLP	Superior	Good	Fair
FPGA	TLP/PLP	Superior	Superior	Bad
Many core	GP/DLP/TLP/PLP	Good	Superior	Good

※GP: General Purpose, IMG: Image processing, DLP: Data Level Parallelism, TLP: Task Level Parallelism, PLP: Pipeline Level Parallelism

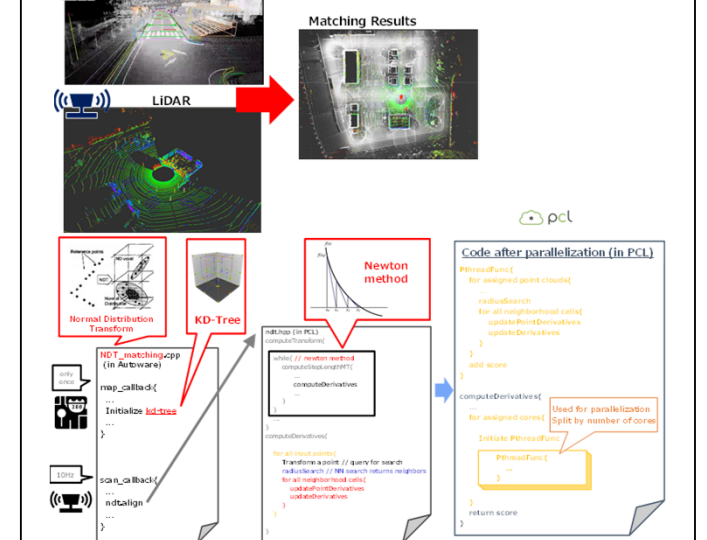
Major Outcomes/Progress



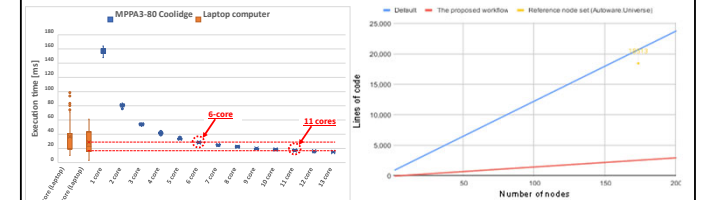
* Except for the standard library, Porting may be required



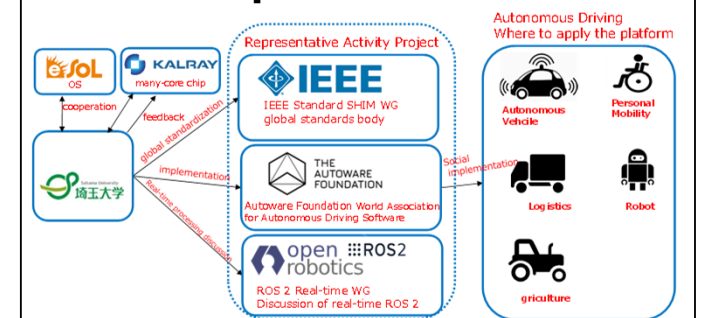
Parallelization of Self-Localization



Parallelization Results Lines of Code Generated



Broader Impact & Future Goals



Research results will be released as **open source**
International collaboration already established