Software Platform for Low-Consumption Autonomous Mobility

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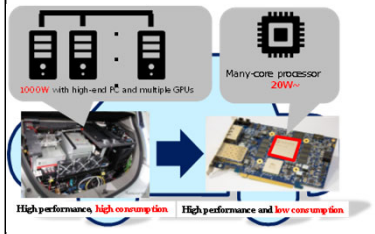
Project Challenge

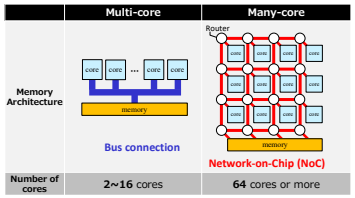
Many-Core Processor Utilization in Mobility

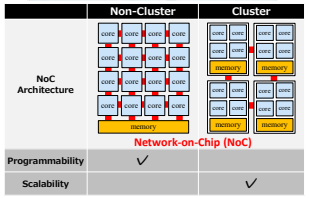
- Building out a robust middleware infrastructure compatible with **ROS 2 for many-core processors**
- Establishing **a model-based development** paradigm for many-core environments that balances **parallel computing** with **high productivity** demands

Intellectual Merit

The construction of ICT infrastructure software that makes effective use of **many cores** and takes into account the **scale**, **power saving**, and **real-time performance**





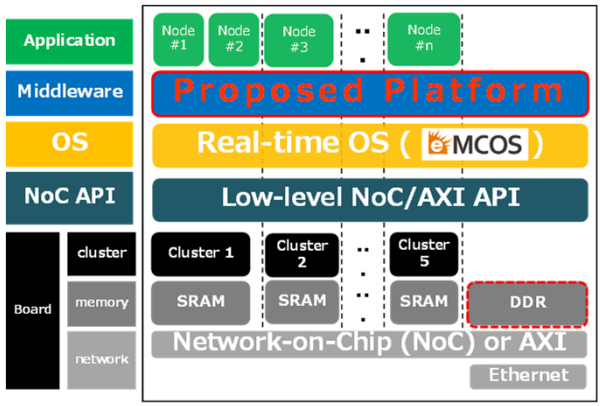


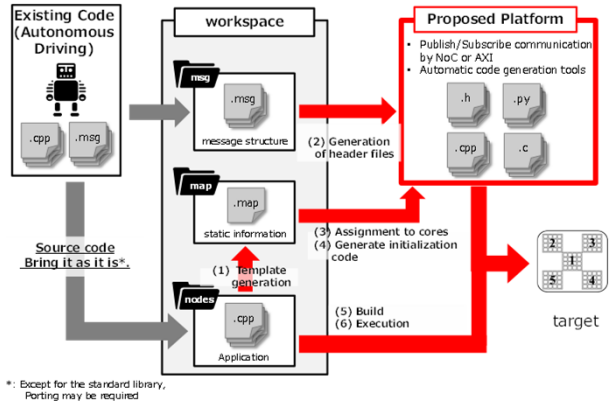
Hardware Resource Comparison (CPU/GPU/FPGA/Many core)

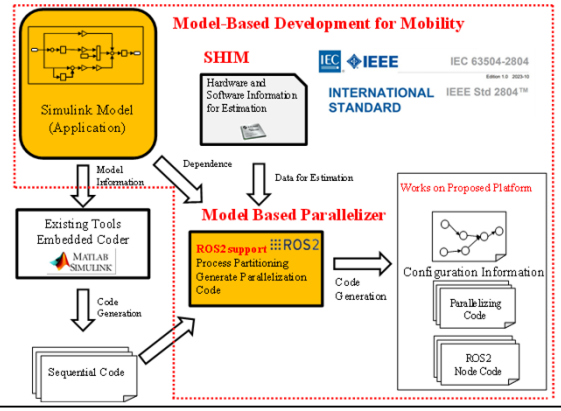
Hardware Resource	Purpose	Peak Performance	Energy Efficiency	Productivity
CPU	GP	Bad	Fair	Superior
GPU	IMG/DLP	Superior	Good	Fair
FPGA	TLP/PLP	Superior	Superior	Bad
Many core	GP/DLP/TLP/PLP	Good	Superior	Good

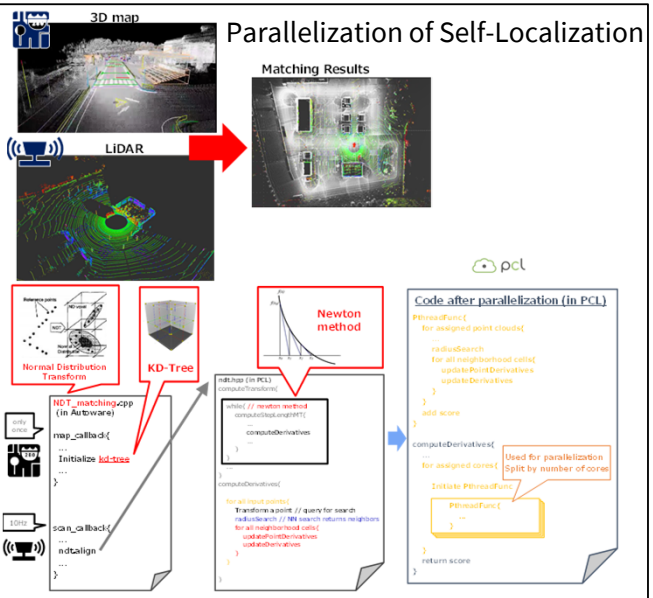
※GP: General Purpose, IMG: Image processing,
DLP: Data Level Parallelism, TLP: Task Level Parallelism,PLP: Pipeline Level Parallelism

Major Outcomes/Progress

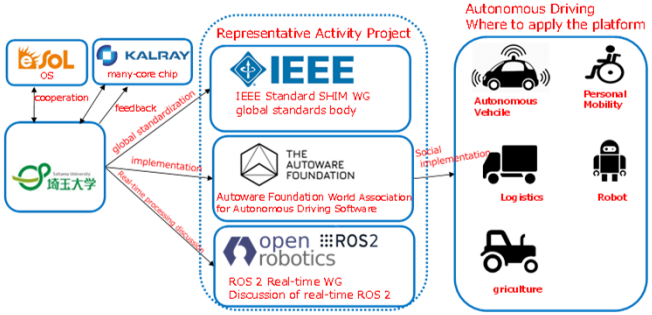








Broader Impact & Future Goals



Research results will be released **as open source**
International collaboration already established